HETEROSTRUCTURE ACOUSTIC CHARGE TRANSPORT TECHNOLOGY FOR PROGRAMMABLE TRANSVERSAL FILTERS

William J. Tanski, Sears W. Merritt, Donald E. Cullen,
Roger D. Carroll, Emilio J. Branciforte, Robert N. Sacks
United Technologies Research Center, East Hartford, CT 06108
and
William D. Hunt, Georgia Institute of Technology, Atlanta , Georgia 30332

ABSTRACT

Significant progress has been made recently in the development of heterostructure acoustic charge transport (HACT) technology. In this paper the HACT device concept is reviewed, details of the layer structure, monolithic integration, and acoustic performance are discussed, and the performance of transversal filters is presented.

A transversal filter 3.35 μsec long (1 cm) with 480 taps and charge transfer efficiency in excess of 0.9999 is described. This is the longest acoustic charge transport device reported to date. Measurements show the thermal dynamic range of the device to be 80 dB, and the spurious free dynamic range is 62 dB, over the 300 kHz bandwidth of the filter.

INTRODUCTION

Advanced communications and radar systems require high-speed, monolithic, signal processors in which the functions of delay and signal storage are integrated on the same chip with conventional electronic gain, summation, and multiplication functions. The HACT device, (1,2), is a unique electronic signal processing element which provides the functions of delay and distributed signal sensing on a GaAs chip which can be monolithically integrated with conventional MESFET electronics. Significant improvements made recently in the design and performance of the HACT device are reported here. Following a brief review of the HACT device concept, the epitaxial layer structure and the MBE growth techniques are described, and the performance characteristics of the latest devices are presented.

The fundamental components of an acoustic charge transport device (both HACT and ACT devices (3,4)) are shown schematically in Figure 1. This structure allows the transport of electron packets in a buried channel in epitaxial layers on a GaAs substrate. The HACT device is similar in function to a conventional charge coupled device (CCD) with the significant difference being the mechanism for longitudinal (direction of SAW propagation) charge confinement and transport. In the acoustic transport device, a traveling surface acoustic wave (SAW)

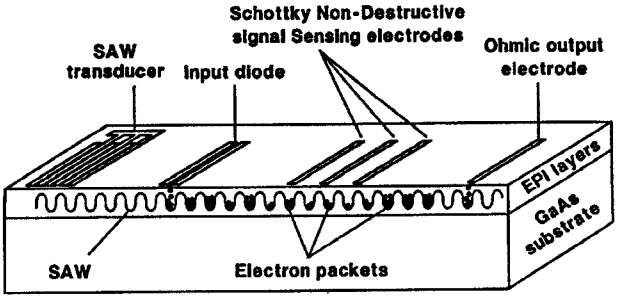

Figure 1.
Simplified schematic of an acoustic charge transport transversal filter showing the primary elements of the device.

potential is generated by the interdigital transducer through the piezoelectric properties of GaAs. The SAW potential is used to collect electrons from the input ohmic contact and to transport these electron packets under the sense electrodes at the SAW velocity of approximately 2864m/sec. This is in contrast to the CCD where a clocking voltage must be applied to an array of electrodes displayed on the surface.

In the HACT device, electrons are injected into the epitaxial layer by means of a diode at the leading edge of the transport channel. The number of electrons formed into each packet is directly proportional to the signal voltage applied to the diode. A key feature of the HACT device is the vertical charge confinement mechansim. In the HACT epitaxial layer structure, shown in Figure 2, the conduction band discontinuities between a layer of GaAs and adjacent barrier layers of $(Al_x,Ga_{1-x})As$ (with x

CH2848-0/90/0000-1107$01.00 © 1990 IEEE

in the range of 0.30) are used to form a potential well in which the charges are confined vertically and transported along the line. This simple charge confinement mechanism is

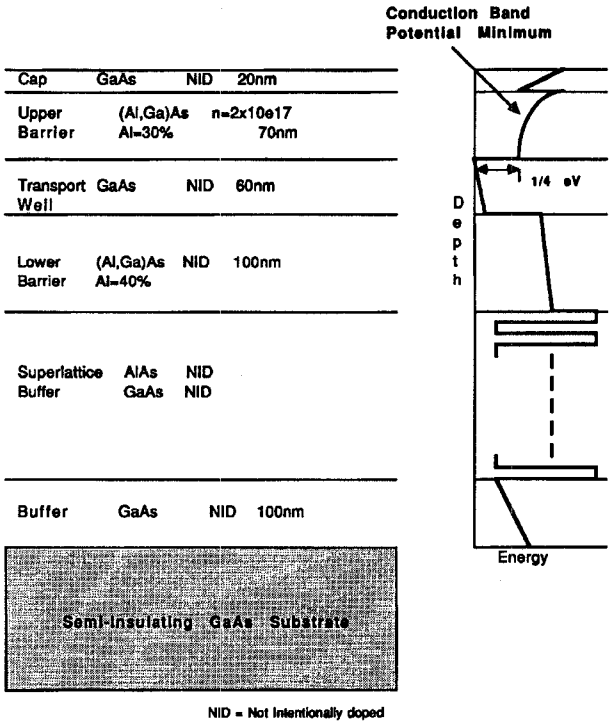

Figure 2.
Epitaxial layer structure and simplified conduction band diagram of the high performance (HACT) devices recently produced.

independent of the clock frequency, it provides for strong coupling to non-destructive sensing (NDS) electrodes (shown on Figure 1) due to the close proximity (within 100 nm) of the charges to the surface, and the epitaxial layers can be grown reliably using Molecular Beam Epitaxy (MBE). The packets are confined in the lateral direction by forming the transport channel on a mesa, or alternatively by ion implant isolation. In the ACT (3,4) structure charges are confined vertically by the parabolic depletion potential in a thick (one half of a SAW wavelength, i.e. 5 μm for a 360 MHz SAW clock), lightly doped, GaAs layer. The layer is depleted by the application of a potential between electrodes on the surface and the bottom of the substrate. In the ACT structure the epitaxial layer thickness is inversely proportional to the clock frequency.

EPITAXIAL LAYER DESIGN AND GROWTH

The HACT device is a large area structure (current active area dimensions are 1 mm by 10 mm) with stringent requirements on the quality of the GaAs in the transport well. The length of the transport channel is determined by the required delay and by the number of sense electrodes needed for a given device function. Defects must be minimized in order to ensure a high degree of charge transfer efficiency (CTE). To put this in perspective, it is necessary to transport charge packets in the range of 10^6 electrons, and not lose more than 100 electrons (a CTE>0.9999) for each transfer of one SAW wavelength.

The epitaxial layer design which has been developed, and which is currently in use, is shown in Figure 2. The objective of the design and growth is to produce a GaAs transport well, in the range of 60 nm thick, with very low levels of dislocations, impurities, oval defects, with low interface roughness at the adjacent barrier (Al,Ga)As layers, and with a sufficiently high barrier potential. The epitaxial layer growth is performed at on an in-house MBE system on a semi-insulating GaAs substrate. The wafer is mounted in the MBE system with an Indium-free holder. There are no specifications on the wafer beyond those required for the fabrication of good quality implanted MESFET's and the growth of high quality epitaxial layers. Dimeric arsenic (As_2), produced by the use of a cracker cell, is used in the epilayer growth process and it has been found that material grown in this manner yields improved HACT device performance.

A thin buffer layer of GaAs is followed by a superlattice buffer of alternating layers of AlAs and GaAs as shown in Figure 2. The details of the superlattice design do not appear to be critical (based on device performance) but the presence of this buffer has demonstrably improved device performance. CTE levels in excess of 0.9999 over 1 cm have been achieved, which was not possible with earlier structures. The lower and upper $(Al_x,Ga_{1-x})As$ barrier layers, with the GaAs layer in between, form the well which has a potential step of about 0.25 eV for 30% Al. The transport well thickness of about 60 nm was chosen to minimize electron-energy quantization effects in the well. The Al concentration in the upper barrier layer has been limited to about 0.30 to facilitate ohmic contact formation. In addition, this upper barrier layer is doped in order to provide electrons needed to satisfy the electronic surface states at the surface. The purposes of the cap layer are to

facilitate ohmic contact formation and to protect the upper (Al,Ga)As barrier from oxidation.

The epitaxial layer quality is determined by visual inspection (noting the size and density of both oval and other defects), by capacitance-voltage plots to determine the carrier concentration as a function of depth, and photoluminescence to gain knowledge of the overall material quality (i.e., levels of microscopic defects such as dislocations and impurities). Photoluminescence data consistently show higher intensity peaks and narrower linewidths for layers with a superlattice buffer, and for layers grown using dimeric arsenic.

HACT/MESFET MONOLITHIC INTEGRATION

HACT devices have been fabricated on wafers with monolithically integrated ion-implanted MESFET's using standard GaAs foundry techniques. The HACT devices were 1.1 μsec long and the MESFET's, with 1 μm gates, had transconductances in excess of 100 mS/mm. HACT device performance was unaffected by the implant anneal, showing that the HACT epitaxial layers are able to withstand the high temperature anneal cycle without degradation. Amplifiers and control circuits will be monolithically integrated with HACT devices in future work.

LASER SCANS OF THE ACOUSTIC PROFILE

The characteristics of the acoustic beam profile were measured on 4.5 μsec HACT devices (containing 720 NDS electrodes) with a knife-edge laser probe system. The purpose of these measurements was to determine if acoustic effects were present which would effect the CTE or other aspects of device performance.

It was found that both the magnitude and phase of the beam profile were flat (+/- 1 dB, +/- 10°) across the HACT mesa at a point 6 mm from the SAW transducer. At 15 mm from the transducer some undulation was observed in the magnitude of the profile which may be due to waveguiding in the NDS array. Scans made along the channel center in the direction of propagation indicated that reflections from the NDS array caused the SAW amplitude to decrease with distance. For devices longer than 6 μsec these reflections must be reduced.

PERFORMANCE OF HACT TRANSVERSAL FILTERS

Figure 3 shows the impulse response of each of the output non-destructive sensing electrodes to charges injected into a single well.

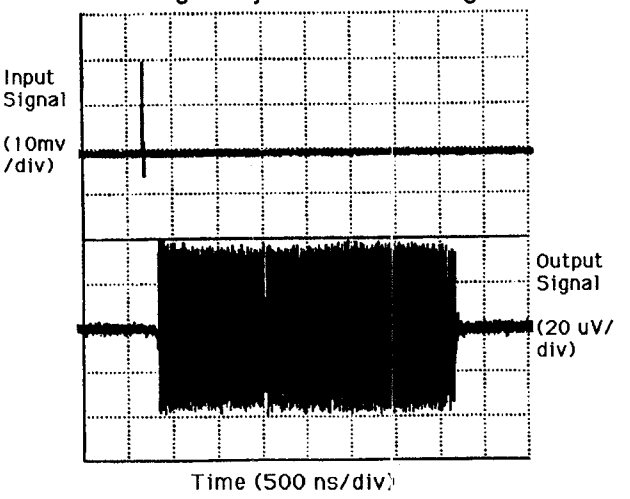

Figure 3.
Impulse response of a 3.3 μsec (1 cm) HACT transversal filter showing the input signal (upper trace) which injects electrons into a single SAW potential well, and the output signal (lower trace) from each of the 480 taps. The CTE is in excess of 0.9999.

The upper trace is the input pulse, and the lower trace is the time domain response of each of 480 sensing taps to the input pulse, as that pulse travels under each tap. The SAW clock frequency was 144 MHz, and the taps were displayed on the surface over 1 cm of length. It is noted that the strength of the output signal from each tap is very nearly the same. Calculations indicate that the CTE for this device exceeds 0.9999, but the exact value is indeterminate due to the slight amplitude undulation. About 1.2 μsec from the leading edge of the tap array there is a gap in the response. This gap is due to a defect found under an electrode in the epitaxial layer. These data show that the design and fabrication techniques are adequate to produce 3.3 μsec charge transport devices, which are believed to be the longest yet produced.

The output power from the 480 tap NDS electrode array, as measured with a spectrum analyzer and a synthesized signal to the input diode, is shown in Figure 4. This response is seen to be a very pure $\sin^2 x/x^2$ pattern with very little distortion. This is in contrast with the high level of distortion frequently seen in SAW device responses which are due to bulk acoustic modes and feedthrough. This low level of distortion in a HACT device frequency response is a unique and potentially useful performance feature. The device exhibited 12 dB of gain at the

passband peak when embedded in the 50 ohm system. The 1 dB compression point occurred at an output power of -8.7 dBm. The third order intercept was calculated to occur at an output power of +2.5 dBm.

Noise in HACT devices is due to thermal fluctuations in the potential across the signal input structure, and is manifested as a variation in the number of electrons in the traveling potential wells even when no signal is present.

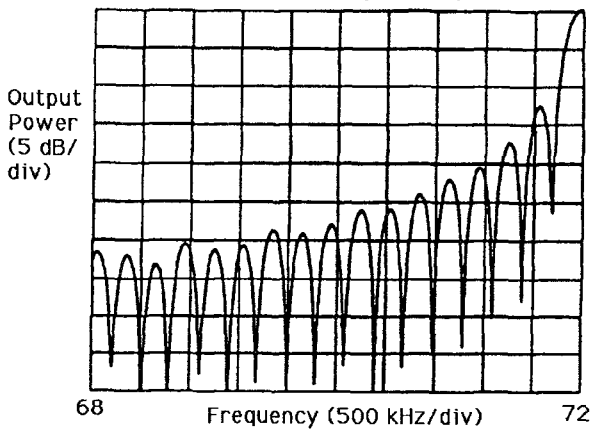

Figure 4
Power spectrum of a 3.3 μsec HACT device. The clock frequency was 144 MHz, and the passband, 300 kHz wide, is at the Nyquist rate of 72 MHz.

The variations in charge load are detected at each of the output electrodes. Assuming a white noise spectrum, the noise power detected at the device output is therefore equal to the noise power generated at the input structure multiplied by the number of output taps.

The noise power density detected by the 480 element output array peaked at -143.9 dBm/ Hz at 72 MHz and exhibited the $\sin^2x/x^2$ power spectrum predicted for the HACT device output structure. The noise power detected by a single tap was calculated to be -170.7 dBm/Hz. This compares favorably to the room temperature thermal noise power spectral density of -173.9 dBm/Hz.

By approximating the filter response as a rectangle about the main response lobe, the calculated noise floor in the 300 kHz bandwidth is -89 dBm. The thermal dynamic range, defined as the ratio of the 1 dB compression point to the noise floor, is 80 dB. The spurious free dynamic range based upon the third order intercept point is 62 dB. Characteristics related to the dynamic range of the HACT device are summarized in Figure 5.

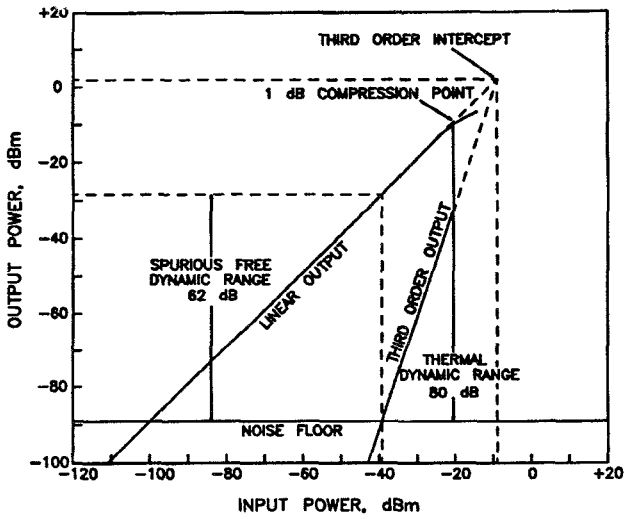

Figure 5
Dynamic range parameters for a HACT device.

SUMMARY

The fabrication, structure, and performance of a 3.35 μsec fixed tap-weight HACT transversal filters, sampled at 144 MHz, is discussed. The absence of amplitude roll-off in the impulse response data indicates that devices with longer integration times are feasible. Acoustic measurements indicate that there is little degradation of the SAW wave. The thermal dynamic range and spurious free dynamic range demonstrated in the device are comparable to those achieved in high quality components used in receivers. HACT devices are fabricated on standard semi-insulating GaAs wafers and monolithic integration of HACT devices and ion-implanted MESFET's has been demonstrated.

REFERENCES

(1) W. J. Tanski, S. W. Merritt, R. N. Sacks, D. E. Cullen,E. J. Branciforte, R. D. Carroll, and T. C. Eschrich, "Heterojunction acoustic charge transport devices on GaAs", Appl. Phys. Lett., vol. 52, no. 1, pp.18-20, 1988.

(2) R. N. Sacks, W. J. Tanski, S. W. Merritt, D. E. Cullen, E. J. Branciforte, and T. C. Eschrich, "Acoustic charge transport in an(Al,Ga)As/GaAs heterojunction structure grown by MBE," J. Vac. Sci. Technol. B, vol. 6, pp. 685-687, 1988.

(3) M.J. Hoskins, H. Morkoc, and B.J. Hunsinger, "Charge Transport by Surface Acoustic Waves in GaAs", Appl. Phys. Lett., Vol. 41, No. 4, August 1982

(4) M.J. Hoskins, "Acoustic Charge Transport in Gallium Arsenide", Ph.D. Thesis, U. of Illinois, 1983.

Acknowledgments

This work was partially funded by the U. S. Army under contract DAAL01-88-C-0863, Mr. Elio Mariani, contract monitor. The authors wish to thank D. W. Eichler for assistance in the epitaxial layer growth, S.K. Sheades for device testing and circuit fabrication, and T. W. Grudkowski and A. G. Foyt for their encouragement and support of this work.